The art of the language VM, or Machine-generating virtual machine code, or Almost zero overhead with almost zero assembly, or My virtual machine is faster than yours

Luca Saiu
positron@gnu.org
http://ageinghacker.net
GNU Project

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About these slides: Copyright © Luca Saiu 2017, 2018, 2022, released under the CC BY-SA 4.0 license. Updated version, last changed on 2022-01-14. The master copy is at http://ageinghacker.net/talks/
These slides are for my presentation at GHM2017.

- You can watch a video recording of my talk: https://audio-video.gnu.org/video/ghm2017 (search for “Jitter”);
- still relevant but 2017 was a few years ago; Jitter has since evolved...
- ...Jitter is now part of the GNU Project: https://www.gnu.org/software/jitter
Introduction and history

My main long-term project is GNU epsilon. It’s a programming language, meant to be efficient, but:

- very “dynamic” in certain execution phases
- written in itself, bootstrapped

— Too slow.

So I wrote a canonical threaded-code VM.

- speedup 4-6x

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- tried techniques from scientific papers (many by Anton Ertl and the other GForth people)
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Why you should care

Interpreters are common:

- programming languages
- application scripting
- shells
- regular expressions...

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Our running example — at first in C

Count down from two billion (here meaning $2 \cdot 10^9$):

```c
int main (void)
{
    long i;
    for (i = 2000000000; i != 0; i --)
        /* Do nothing */;
    return 0;
}
```

...does this program really count down?
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C (with GNU extensions)

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[Demo: the down-counter in a few languages]
You can play with the sources

I will (quickly) show some interpreters written in C.

In case you want to play with the examples yourself, the little programs I’m showing here are on my server:

http://ageinghacker.net/projects/jitter/ghm-2017

These are naïf C programs showing how interpreters work; the C files in c-examples/ are not part of my new project.
How simple interpreters work

The interpreted program is a data structure in memory. "find the next point in the interpreted program, execute it, repeat from start"

How to dispatch [“dispatch”: moving from a VM program point to another]:
- Abstract Syntax Tree (AST) interpreters
- Linear programs
  - switch dispatching
  - direct threading
  - ...

How to access data:
- associative data structures (alists, hash tables)
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- stacks
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A program is an Abstract Syntax Tree data structure in memory: heap-allocated structs and unions with lots of pointers. Each node has an enum field to distinguish its kind.

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Our down-counter as an Abstract Syntax Tree

sequence

assign
do-while

i := 2000000000;
do
  decrement i;
while i != 0;

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Abstract Syntax Tree interpreter: expression

Each complex AST has sub-ASTs: recursion is natural. AST data structures are easy to define in Lisp and ML — in C a little less pretty, but the idea is the same.

```c
long interpret_expr (const struct expr *e, const long *vars) {
    switch (e->expr_case) {
        case expr_variable:
            return vars [e->var_index];
        case expr_constant:
            return e->cnst;
        case expr_is_different:
            return ( interpret_expr (e->sub1, vars)
                      != interpret_expr (e->sub2, vars));
        default:
            error ();
    }
}
```
Abstract Syntax Tree interpreter: statement

```c
void interpret_stmt (const struct stmt *s, long *vars) {
    switch (s->stmt_case) {
    case stmt_sequence:
        interpret_stmt (s->sub1, vars);
        interpret_stmt (s->sub2, vars);
        break;
    case stmt_assign:
        vars [s->var_index] = interpret_expr (s->assigned_expr, vars);
        break;
    case stmt_decrement:
        vars [s->var_index] --;
        break;
    case stmt_dowhile:
        interpret_stmt (s->body, vars);
        if (interpret_expr (s->guard, vars))
            interpret_stmt (s, vars);
        break;
    default: error ();
    }
}
```
AST interpreter performance

- pointer chasing (load latency $\sim 3\tau$ on L1d hit!)
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A good language to interpret

What is normally called a language “Virtual Machine” is an interpreter for a lower-level **linear** program:

- the program to interpret is stored as a contiguous **array** in hardware memory
- no nesting: no statements with sub-statements or expressions with sub-expressions
- no expressions, no variables
- assembly-like feel: registers or stacks, explicit jumps

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The down-counter as a linear program to be interpreted

```plaintext
set 2000000000, %r0
set -1, %r1
$L1: add %r0, %r1, %r0
bnz %r0, $L1
end
```

- VM registers are an array in hardware memory.
- The VM program is an array in hardware memory.
- Only the interpreter’s automatic C variables are in hardware registers.
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```
insn_set
2000000000
0
insn_set
-1
1
insn_add
0
insn_bnz
0
insn_end
```

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**Example AST**

```
insn
  regs
    VM %r0
    VM %r1
    VM %r2
    VM %r3
    VM %r4
```

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What’s the C type of `insn_set`, `insn_add`, `insn_bnz`, `insn_end`?

- It’s an `enum insn`: essentially an integer.
- There are also pointers `in` the VM program array from an element to another...
- Linear-program interpreters work best with word-sized data: objects as wide as a hardware register. `unions` are useful for this:

```c
union value {
    enum insn in;
    long i; // or another integer type of the right width
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This interpretation style is called `switch` dispatching.

[switch dispatching: C source and demo]
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Problems with `switch`-dispatching

Performance of a `switch`-dispatching interpreter:

- `switch` is somewhat inefficient (range checking)
- The CPU branch target predictor can’t work well: one jumping instruction with many possible targets, complex repetition patterns.
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GCC introduced the C extension called **computed goto** or **labels-as-values**:

- The expression `&& label`, of type `void *`, evaluates to the address of the hardware machine instruction where the labeled code begins; you can store the address and jump to it later.
- The statement `goto *expr` jumps to the result of the evaluation of `expr`.

We can use pointers to native code instead of enums in the VM program, at the beginning of every VM instruction. This is called **direct-threaded code** (*nothing to do with multi-threading*).
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The down-counter program for a direct-threaded VM

Inspn | regs
---|---

2000000000

0
-1
1
0
VM %r0
VM %r1
VM %r2
VM %r3
VM %r4

Compiled hardware machine code for set
Compiled hardware machine code for add
Compiled hardware machine code for bnz
Compiled hardware machine code for end

Instead of an enum identifier each VM instruction in the VM program begins with a pointer to its native code.

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**Direct-threaded interpretation**

In **direct threading**:

- interpreting the VM instruction pointed by a C pointer `p` is trivial: `goto *p;`
- there’s no switch
- no infinite loop or jump to a shared conditional: each VM instruction “falls thru” to the next by jumping:
  - move `insn` forward
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[C source and demo]
Direct-threaded fallthru (nop): diagram

The zero-argument VM instruction \texttt{nop} does nothing and just falls thru to the next instruction.
The jump destination address is pointed from memory (red arrow). The green arrow is the pointer \texttt{insn}, already in a hardware register.

There is nothing between the code pointer for \texttt{nop} and the code pointer for the next VM instruction since \texttt{nop} has no arguments.
Direct-threaded fallthru (\texttt{nop}): code

Here’s the source for the VM instruction \texttt{nop} in the direct-threading interpreter:

\begin{verbatim}
GNU C

label_nop:
    insn ++;  // No args to skip, just the code pointer
    goto * insn->label;

compiled (x86_64)

movq 8(%rax), %rdx # insn is in %rax; load (insn + 1)->label
addq $8, %rax  # advance insn to the next instruction
jmpq *%rdx     # jump to the address we loaded before

GCC has put \texttt{insn} in the hardware register \%rax. The load (\texttt{movq} on x86_64) reads the cell below the green arrow head, at 8(\%rax). The hardware register \%rdx is a temporary, holding the address where to jump.
\end{verbatim}
Here’s the source for the VM instruction `nop` in the direct-threading interpreter:

```c
label_nop:
    insn ++; // No args to skip, just the code pointer
    goto * insn->label;
```

```assembly
movq 8(%rax), %rdx  # insn is in %rax; load (insn + 1)->label
addq $8, %rax       # advance insn to the next instruction
jmpq *%rdx          # jump to the address we loaded before
```

GCC has put `insn` in the hardware register `%rax`. The load (`movq`) reads the cell below the green arrow head, at `8(%rax)`. The hardware register `%rdx` is a temporary, holding the address where to jump.
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GCC has put `insn` in the hardware register `%rax`. The load (`movq` on x86_64) reads the cell below the green arrow head, at `8(%rax)`. The hardware register `%rdx` is a temporary, holding the address where to jump.
The \texttt{b} VM instruction takes a label as its parameter: the next VM program slot after \texttt{b}'s code pointer points to the beginning of the target instruction (another slot in the program containing a code pointer).
Direct-threaded unconditional branch (b): code

The (one-argument) VM instruction b in the direct-threading interpreter:

```c
label_b:
    insn = insn[1].p;
    goto * insn->label;
```

*compiled (x86_64)*

```c
movq 8(%rax), %rax  # load jump destination from *(insn + 1)
jmpq *(%rax)        # jump indirect via memory: another load
```

The first instruction loads the next insn, still pointing within the program array. The jump-via-memory instruction chases a pointer from it and obtains a pointer into a “blue” box, the hardware instruction where to jump where the target VM instruction begins.
Direct-threaded unconditional branch (b): code

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**GNU C**

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The first instruction loads the next insn, still pointing within the program array. The jump-via-memory instruction chases a pointer from it and obtains a pointer into a “blue” box, the hardware instruction where to jump where the target VM instruction begins.
Direct-threaded conditional branch (bnz)

The two-argument VM instruction bnz in the direct-threading interpreter:

```c
label_bnz:
    if (regs[insn[1].i] != 0)
        insn = insn[2].p;
    else
        insn += 3;
    goto * insn->label;
```

compiled (x86_64, simplified)

```assembly
movq 8(%rax), %rdx
cmpq $0, -256(%rbp,%rdx,8)
je L
movq 16(%rax), %rax # Like b
jmpq *(%rax)
L: addq $24, %rax     # Fallthru
    jmpq *(%rax)
```

Check the condition; if false skip past (je) unconditional branch code, and into fallthru dispatch code.

Lots of hardware branches, depending on memory and on each other.

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Direct-threaded conditional branch (\texttt{bnz})

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**GNU C**

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  else
    insn += 3;
  goto * insn->label;
```

**compiled (x86_64, simplified)**

```assembly
    movq  8(%rax), %rdx
    cmpq $0, -256(%rbp,%rdx,8)
      je    L
    movq  16(%rax), %rax   # Like \texttt{b}
    jmpq  *(%rax)
L:    addq $24, %rax      # Fallthru
    jmpq  *(%rax)
```

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Lots of hardware branches, depending on memory and on each other.
Direct threading dispatch performance

slow?
The real question is whether we can do better, and where the bottleneck is.

Is branching/fallthru the only source of inefficiency?

[Demo: quick timing against switch-dispatching]
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Let’s look at how the VM instruction `add %r3, %r0, %r1` is represented in the VM program and what it needs to do in terms of hardware “operations”:

- read VM register indices (load from insn[k] obtaining 3, 0, 1)
- read VM input register contents from the VM register array using input indices (load VM register elements %r3, %r0 using indices 3, 0)
- do the actual sum
- write result into VM register array (store into VM %r1 using index 1)
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Let’s look at how the VM instruction `add %r3, %r0, %r1` is represented in the VM program and what it needs to do in terms of hardware “operations”:

- **Compiled hardware machine code for add**
- **Compiled hardware machine code for the following instruction**

- **insn**
  - **regs**
    - VM %r0
    - VM %r1
    - VM %r2
    - VM %r3

- **read VM register indices** (load from insn[k] obtaining 3, 0, 1)
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(Direct-threaded) VM add: “fundamental”/RISC operations

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  - do the actual sum
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  - write result into VM register array (store into VM %r1 using index 1)
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Compiled hardware machine code for add

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- ** insn **
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- **Compiled hardware machine code for add**
- **Compiled hardware machine code for the following instruction**

- **insn**
  - regs
    - VM %r0
    - VM %r1
    - VM %r2
    - VM %r3

- **Compiled hardware machine code for add**
  - insn
  - 3
  - 0
  - 1

- **Compiled hardware machine code for the following instruction**

- read VM register indices (load from insn[k] obtaining 3, 0, 1)
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- fallthru: `increment-load-jump`, as always
The VM instruction add (here direct-threaded), compiled

Is our three-operand add simple and fast, at least on a CISC?

```c
GNU C

label_add:
    regs[insn[3].i]
        = ( regs[insn[1].i]
            + regs[insn[2].i]);
    insn += 4;
    goto * insn->label;
```

- The actual addition costs **only one** hardware instruction (the second `addq` [which also includes one memory access]).
- Fallthru to the next VM instruction: **three** hardware instructions (`increment-load-jump`).
- The other **five** hardware instructions only serve to access VM registers (and on RISCs it’s even worse).
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Is our three-operand add simple and fast, at least on a CISC?

**GNU C**

```c
label_add:
    insn += 4;
    goto * insn->label;
```

**compiled (x86_64, simplified)**

```assembly
movq 8(%rax), %rsi
movq 16(%rax), %rdx
addq $32, %rax
movq -8(%rax), %rcx
movq -256(%rbp,%rdx,8), %rdx
addq -256(%rbp,%rsi,8), %rdx # +
movq %rdx, -256(%rbp,%rcx,8)
movq (%rax), %rdx
jmpq *rdx
```

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insn += 4;
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The VM instruction add (here direct-threaded), compiled

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```
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label_add:
insn += 4;
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- the actual addition costs only one hardware instruction (the second addq [which also includes one memory access]).
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compiled (x86_64, simplified)

```
movq 8(%rax), %rsi
movq 16(%rax), %rdx
addq $32, %rax
movq -8(%rax), %rcx
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The VM instruction add (here direct-threaded), compiled

Is our three-operand add simple and fast, at least on a CISC?

```c
void label_add:
    insn += 4;
    goto * insn->label;
```

- the actual addition costs only one hardware instruction (the second addq [which also includes one memory access]).
- Fallthru to the next VM instruction: three hardware instructions (increment-load-jump).
- The other five hardware instructions only serve to access VM registers (and on RISCs it’s even worse).
In the C code for VM instructions we access VM register contents with expressions such as \( \text{regs}[idx] \), where \( idx \) is usually \( \text{insn}[k].i \) for some constant \( k \).

Reading \( \text{insn}[k].i \) into \( idx \) costs one load instruction (register plus a known constant offset). Loading \( \text{regs}[idx] \) is more delicate: the address to load from is

\[
\text{regs} + idx \cdot w
\]

where \( w \) is the word size in bytes (4 on 32-bit machines, 8 on 64-bit machines). The multiplication requires a separate shift instruction on most RISC machines [plus possibly yet another instruction for summing \( \text{regs} \) and \( (idx \cdot w) \): needed on RISC-V, MIPS, Alpha].

Shifting at run time is silly: instead of keeping VM register indices in the VM program we can keep VM register offsets from \( \text{regs} \), or in other words we can keep pre-shifted register indices.
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(Direct-threaded) VM add: register indices and shifts

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(Direct-threaded) VM add: operation dependency graph

“\(a \rightarrow b\)” means that \(a\) uses the result of \(b\), so \(b\) is executed before \(a\). Thick arrows mean high latencies (\(\sim 3\tau\)).

[Register index shifts shown, offset sums to regs base not shown]

Two long dependency chains, each including two loads:
\(load \leftarrow shift \leftarrow load \leftarrow add \leftarrow store\). \(\sim 6\tau\) latency just from the loads, with ideal Instruction-Level Parallelism! In practice it will be worse.
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[Register index shifts shown, offset sums to regs base not shown]

```
load idx 0
  ↑
shift idx 0
  ↑
load VM reg 0
load idx 1
  ↑
shift idx 1
  ↑
load VM reg 1
load target
  ↑
jump
add
  ↘
update insn
store VM reg 2
  ↑
shift idx 2
```

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[Register index shifts shown, offset sums to regs base *not* shown]

```
load idx 0  \uparrow
  shift idx 0  \uparrow
    load VM reg 0

load idx 1  \uparrow
  shift idx 1  \uparrow
    load VM reg 1

load target  \uparrow
  jump

add
  update insn

store VM reg 2
  shift idx 2  \uparrow

Two long dependency chains, each including two loads:
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(Direct-threaded) VM \( b \): operation dependency graph

```
load instr
    ↑
load code pointer
    ↑
jump
```

Longest (and only) dependency chain \( load \leftarrow load \leftarrow jump \). A VM unconditional branch has latency similar to a VM \( \text{add} \); a VM \( b \) can easily be faster than a VM \( \text{add} \) if the hardware branch target predictor does its job.

VMs and hardware machines can have very different performance profiles.

[I’ve understood, too late to make the change before the GHM, that this is optimizable. Can you see how? Hint: \( b \) can have two arguments instead of one, at least in the memory representation of the program.]
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Stack-oriented VM instructions replace the top few elements of a stack with the result of an operation. For example `stack_add` (zero arguments) could pop two elements (say, 5 and 6) from the stack and push their sum (11). This idea is about using stacks instead of VM registers, not just call stacks.

The authors of [Shi et al., 2005], in other works as well, argue from experimental data that direct-threaded register VMs are faster than direct-threaded stack VMs (same model I’m presenting here, stack code machine-translated to VM-register code with optimizations).

Unfortunately it’s difficult to replicate their measurements. I wonder if their results still hold today, with our proportionally slower L1d caches and better branch predictors. [Still, stack code takes more instructions to do the same work, today like in 2005] I’ll explain why I have doubts.
What if we used a stack instead of VM registers?

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Luca Saiu
http://ageinghacker.net
The art of the language VM — GNU Hackers’ Meeting 2017
Naïve stack implementation

Suppose the VM has a **stack** in a hardware memory array, with a **top-of-stack pointer** in a hardware register. This is a zero-argument **stack_add** VM instruction:

```c
label_stack_add:
    top [-1] = top [-1] + top [0];
    top --;
    /* Fallthru code omitted, same as always. */
```

Before:

```
    top
    5
    6
```

After:

```
    top
    5
    11
```

Two (independent) loads, one store. This looks better than our VM-register add: constant offsets from **top**, no index/offset loads.
Naïve stack implementation

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```c
label_stack_add:
    top [-1] = top [-1] + top [0];
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```

Before:

- `top`: 5
- `top`: 6

After:

- `top`: 5
- `top`: 11

Two (independent) loads, one store. This looks better than our VM-register add: constant offsets from top, no index/offset loads.
Suppose the VM has a stack in a hardware memory array, with a top-of-stack pointer in a hardware register. This is a zero-argument stack_add VM instruction:

```
GNU C
label_stack_add:
  top [-1] = top [-1] + top [0];
  top --;
  /* Fallthru code omitted, same as always. */
```

Before:
```
<table>
<thead>
<tr>
<th>top</th>
<th>5</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>6</td>
</tr>
</tbody>
</table>
```

After:
```
<table>
<thead>
<tr>
<th>top</th>
<th>5</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>11</td>
</tr>
</tbody>
</table>
```

Two (independent) loads, one store.
Naïve stack implementation

Suppose the VM has a stack in a hardware memory array, with a top-of-stack pointer in a hardware register. This is a zero-argument stack_add VM instruction:

```c
label_stack_add:
    top [-1] = top [-1] + top [0];
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```

Before:
```
   top
   5
   6
```

After:
```
   top
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   11
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Two (independent) loads, one store. This looks better than our VM-register add: constant offsets from top, no index/offset loads.
Top-Of-Stack (TOS) optimization

We can do even better: keep the VM top stack element in a hardware register (the rest of the stack still in a hardware memory array), and an under-top pointer in a second hardware register.

GNU C

```
label_stack_add:
tos = tos + undertop [0];
undertop --;
/* Fallthru code omitted, same as always. */
```

Before:

```
tos = 5
undertop
   6
```

After:

```
tos = 11
undertop
   6
```

Only one load. Other VM instructions working only on the TOS (for example stack_increment) require zero loads.
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```

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(Direct-threaded) TOS-optimized stack_add: operations

This includes the fallthru operations (*update insn*, *load target*, *jump*).

```plaintext
load target
    ↑
  jump   update insn   update under-top ptr.
```

Very “flat”-looking graph with short dependency chains (max length 1). Not many operations.
(Direct-threaded) TOS-optimized stack_add: operations

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\[
\begin{align*}
\text{load target} & \quad \uparrow \\
\text{jump} & \quad \text{update insn} \\
\text{add} & \quad \text{load under-top} \\
\text{update under-top ptr.} & \quad \uparrow
\end{align*}
\]

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Nothing of what you saw up to here is new except for the removal of register *index shifts*, a minor optimization.

I want to make my VMs faster. In order of priority I need to:

- optimize VM register (and immediate argument) access [new]
- optimize fallthru [I learned the idea from [Ertl and Gregg, 2004], which builds upon previous work]
- remove insn and the VM program in memory [conceptually easy]
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VM registers should not be in **hardware memory**. I want them in **hardware registers** (as long as they fit).

The problem: every time I do anything with

```
regs[e]
```

and the value of `e` isn’t known at compile time I lose. GCC can’t put any `regs` element in a specific hardware register, while there is even one `regs[e]` expression with unknown `e` — reading or writing.

The solution: never use `regs[e]` with a non-constant `e`; or even split `regs` into scalar variables `reg_0, reg_1, reg_2, ...` and never take the address of those variables: writing “& regs_\(i\)” is forbidden for every \(i\).
Optimizing VM register access

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Let's look at a VM instruction such as `add`

[Here with register indices rather than offsets, just for simplicity: same point]

**GNU C**

```c
label_add:
    insn += 4;
    goto * insn->label;
```

Here `regs` is (always) indexed with `insn[k].i`, an index coming from the interpreted program!

And this pattern is very common across VM instructions.

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A radical solution: forbid register indices/offsets as VM instruction arguments.

Remove the VM instruction `add` taking three index/offsets arguments from the interpreter. Instead there will be many specialized VM instructions:

```
add/%r0/%r0/%r0,
add/%r0/%r0/%r1,
add/%r0/%r1/%r0,
add/%r0/%r1/%r1,
add/%r1/%r1/%r1,
add/%r0/%r0/%r2,
```

... Every possible combination.

Specialized instructions have no register-index/offset arguments; the specializations of our example’s `add` have all zero arguments.
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Remove the VM instruction `add` taking three index/offsets arguments from the interpreter. Instead there will be many *specialized* VM instructions:

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- `add/%r0/%r0/%r1`,
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- `add/%r0/%r1/%r1`, ...
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*Every possible combination.*

Specialized instructions have no register-index/offset arguments; the specializations of our example’s `add` have all *zero* arguments.
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Specialized instructions have no register-index/offset arguments; the specializations of our example’s add have all zero arguments.
Bear with me

Yes, I know that you have objections at this point.

Please give me one minute. I will address them.
Where am I going?

Specialization is **not manageable** in human-written code:

- very long and redundant code
- fragile with respect to **trivial details** [how many programs slot to skip for fallthru? The number depends on how many arguments are VM registers]

The solution is machine-generating C code.

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The art of the language VM — GNU Hackers’ Meeting 2017
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The project takes shape

The new software I’m presenting is a code generator, automatically emitting C code for a VM from a human-written specification. Like Bison, and even more like Vmgen [Ertl et al., 2002], [Ertl, 2008].

- user-provided C code snippets for each unspecialized instruction
- convenient automatically-defined CPP macros to refer to (pre-specialization) arguments, and more
- fallthru code implicit for every VM instruction, automatically added by the generator

A VM instruction specification from the “Uninspired” VM (edited)

```c
instruction add (?R, ?R, !R)
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    UNINSPIRED_ARGN2 = UNINSPIRED_ARGN0 + UNINSPIRED_ARGN1;
  end
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Making VMs **general**:

- VM **registers**, or **stacks** (TOS-optimized or not), **both**, anything else implemented by the user
- user-specified **data types** (register classes: for example integer/pointer, floating point, vector, ...)
- several possible **dispatching models**
  - switch-dispatching, direct threading, other models I’ll show later;
  - different performance profiles, identical behavior!
  - lots of **#ifdefs** in the generated C code; choose dispatching model by compiling with **-DDIRECT_THREADING**, ...  
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Making VMs portable with respect to different CPU architectures (also important for political reasons: free hardware as a prerequisite for privacy)

- Using C with as little assembly as possible, and not in user code (the assembly part is VM-independent, and already provided)
- Even that little assembly is optional, only for better performance
- VMs behave identically, with or without assembly support
- Direct threading with specialization is as portable as GCC switch-dispatching even more portable (no goto *) (not yet implemented, but trivial)
- Compiled VMs work comfortably even on “small” machines (32MB RAM is plenty; probably 8 or even 4MB is enough)
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- driver with command-line options (main with convenient GNU command-line support for debugging and benchmarking)
- frontend: VM program parser and printer
- cross-compilation support
- disassembly to native or (via qemu-user) cross-code
- testsuite (even cross-, via qemu-user)

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Along with the generated code you get:

- **C API** for dynamically generating and executing VM programs from your application
- **driver with** command-line options (**main** with convenient GNU command-line support for debugging and benchmarking)
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VM specialized instructions: combinatorial explosion?

If we have $n$ registers and $m$ instructions (for example) all taking 3 register indices as arguments, specialized instructions are $m \cdot n^3$.

Yes, there are practical limits on how many VM registers of this kind you can have.

There are ways to reduce this growth and some optimizations I haven’t implemented yet, but compiling a machine-generated VM is heavy. GCC can use GBs of RAM and take minutes to run when VM registers are many.
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Limiting combinatorial explosion

Some specialized instructions are useless or can be normalized:

- For example, addition is commutative: add/%r0/%r1/%r2 and add/%r1/%r0/%r2 do the same work, and we can keep only one. This halves the number of (commutative) specialized instructions.

- We can also rewrite every specialized instruction such as add/%ri/%rj/%rk into a two-specialized-instruction sequence
  - copy/%rj/%rk
  - add/%ri/%rk/%rk

whenever j ≠ k. [This is correct because add writes its third argument, but doesn’t read it.] This rewrite can cut the number of specialized instructions from \( m \cdot n^3 \) to \( m \cdot n^2 \).

Every specialized instruction which is not a rewrite target “doesn’t exist”.

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What I’ve outlined can be expressed as a rewriting system.

Which rewrites are valid depends on the properties of each specific instruction: such properties must be declared by the user in her VM specification, and cannot in general be inferred.

I’ve not fully implemented rewriting yet, even if the parser recognizes a preliminary syntax. I want a rule-based system which is expressive enough to limit growth, and also to perform a few optimizations in the VM program [for this reason I will implement rewriting on unspecialized VM instructions]

Some manual tests have convinced me that with fewer useless VM instructions GCC will do a better job of allocating registers for those which remain. Implementing rewriting is high-priority.

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Combinatorial explosion and stack-based instructions

Do we have the same combinatorial explosion problem with stack-based instruction?

- No. The unspecialized VM instruction add_stack has zero arguments, and only one specialization.
- More in general implied operands limit combinatorial explosion, even with registers. Example: special-purpose registers: mul and div could always write to the same destination register . . .
- Rewrite rules are an easy and powerful way of optimizing stack code.

Example:

```
stack_push 10
stack_plus

→

stack_plusi 10
```

We’ll see how effective this is after I implement rewriting.
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Is VM specialization worth the trouble?

Remove every access to regs with a non-constant index from the interpreter. Then:

(Macro-expanded) GNU C

```c
label_add_r0_r1_r1:
    regs[1] = regs[0] + regs[1];
    insn ++; // skip code ptr. only
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Now regs indices are constants (different in every specialization):

compiled (x86_64)

```assembly
addq $8, %rax
addq %rbx, %rcx
jmpq *(%rax)  # Jump via memory
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Much better than the unspecialized version!

Here GCC has kept the VM register %r0 in the hardware register %rbx and the VM register %r1 in the hardware register %rcx.

[When there aren’t enough hardware machine registers GCC will allocate some VM registers on the C stack, at a known offset from the C stack/frame pointer: still faster than without specialization.]
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More on specialization: slow VM registers

There’s a limit to the number of VM registers we can use for generating specialized instruction. However, for convenience and expressiveness, we can also, optionally, provide an unlimited number of additional VM registers, less efficient to access.

We call the VM registers on which we specialize fast registers, and the others slow registers. Slow registers are implemented as a (separate) array in hardware memory, exactly like pre-specialization VM registers, pointed by slow_regs.

The distinction between fast and slow registers is transparent:

A VM instruction specification from the “Uninspired” VM (edited)

```plaintext
instruction add (?R, ?R, !R)  # Each ‘R’ can be fast or slow
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The same VM instruction can **indifferently use fast or slow VM registers**, or **mix them together**, according to each specialization:

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label_add_r0_rR_r0:
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The generator always encodes slow VM register arguments as pre-shifted offsets from `slow_regs` within the VM program (here `insn[1].i`).

Reading a VM slow register value still takes two inter-dependent loads.
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The same instruction can also be made to access either a VM register or a literal at some position:

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Compiled (x86_64)

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Good!

Here GCC emitted `$1` as a硬件 instruction immediate. This code reads L1d only in the fallthru part.

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VM operand access is now fast in the common case

[solved!]

[ Little demo of the Uninspired VM, with direct-threaded dispatching and specialization for fast operand access ]
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The next bottleneck

We have solved the problem of operand access in the common case.

The interpreter bottleneck has moved: now the problem is dispatching.

- the fallthru code at the end of the typical VM instruction now takes longer than the part doing useful work.
- VM branches are less common than falling thru in real-world programs (the down-counter example is not representative)
- ...so let's not think about VM branches yet
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All VM instructions but unconditional branches end with slow fallthru code. We want to remove it.

The solution is copying compiled specialized VM instruction code sequences one after another, concatenating them into hardware machine-code basic blocks. Then each VM instruction in the block automatically “falls thru” into the next.

A code pointer is only needed at the beginning of each basic block.

I call this dispatching style minimal threading: it’s an optimization of direct threading.
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The sub/%r1/%r0/%r1 VM instruction doesn’t touch L1d or even insn.
The add/%r0/nR/%r1 VM instruction has 7 as its residual literal argument on
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VM instruction replication challenges

Replicating code by itself is not hard [but see Bruno’s point on slide 61]:

- allocate executable memory with `mmap`
- copy machine code for VM specialized instructions into the executable space, delimited by label-as-value pointers.

We have to call GCC with the right options to prevent disasters:
- PC-relative memory accesses or calls.
- non-PIC code
- at least `-fno-reorder-blocks`, `-fpic` mandatory

More subtly, GCC needs to keep its register-allocation compatible across the code for every VM specialized instruction.
- a few tricks: jumps (unreachable in replicated code) at the end of specialized instruction code, jumping to a C jump with a destination unknown to GCC (`volatile`, no-code inline asm with constraints).
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More VM instruction replication challenges

Global variable/function references are a problem (on most architectures), but given their names in C the generator can define macros to have them accessed thru a hidden stack-allocated structure — convenient for C code snippets.

VM specification

```
wrapped-globals
  printf
  printfixnum_format_string # String literals are dangerous!
end

wrapped-functions
  printf
  rand
  xmalloc
end
```

Since when replication is enabled we are already relying on another GCC extension we can afford `typeof` as well in the generated code, to free the user from the need of declaring types.
Minimal threading

Minimal threading is delicate but requires no assembly (unless `__builtin___clear_cache` fails to invalidate L1i, as I saw happen on powerpc).

Very portable: minimal threading is currently tested and working on aarch64, alpha, arm, i386, mips, powerpc, s390, sparc, x86_64 (either endianness, either bitness) — and it probably works on many more architectures. It currently fails on sh4, which relies heavily on PC-relative loads.

Minimal threading does require `mmap`, which isn’t a problem on GNU systems. [After my talk Bruno Haible taught me a technique I didn’t know for working around the restrictions of $W \oplus E$ systems, using two `mmap` mappings; still workable, but I admit that this will add some complexity]

A good dispatching model for most architectures. Where not supported (right now on sh4) the user can always revert to direct threading, lower-performance but as portable as GCC.
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Next bottleneck: VM branches

With minimal threading we have mostly [we still need to increment insn for VM instructions with residual arguments] eliminated fallthru overhead.

The next bottleneck to eliminate is VM branching — fallthru overhead will also go away completely as a side effect.

- All VM branching overhead comes from the direct-threading convention of having VM program slots contain pointers to executable code.
- Moreover residual literals and slow register offsets are also loaded from the VM program in memory, which is usually suboptimal.

Why having the VM program as a data structure in memory at all?
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Introducing the last and most efficient dispatching mode, no threading.

The idea: do away with the VM problem as a data structure, and only keep the replicated executable code.

At this point we need some architecture-specific assembly code:
- Residual literals must be materialized into hardware registers or memory, since there is no program to load them from
  - Small hand-written assembly routines, to be patched with literals...
  - ...copied before the beginning of each VM specialized instruction code needing residuals.
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Without the VM program there is no longer need for `insn` either — not even in a hardware register.

- The VM instruction pointer is the same as the hardware instruction pointer (`%rip` on x86_64): native hardware branches!

- Branching via a hardware register is easy in GNU C and requires no assembly: `goto *`...

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No-threading dispatch: label arguments

Label literals, as wide constants, are painful to load on RISCs and also force the CPU to jump thru a register or memory.

- We want to replace jumps in C code snippets with the appropriate hardware machine instructions—also in the conditional case.
- Difficult, as jumps may occur anywhere within compiled C code.

Solution: provide predefined macros VMPREFIX_BRANCH_FAST, VMPREFIX_BRANCH_FAST_IF_LESS_THAN, VMPREFIX_BRANCH_AND_LINK_FAST, ... expanding to patch-ins:
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What a patch-in is

Every patch-in use generates an sequence of 0x0s in compiled code, of the right length for the missing hardware instruction(s) to be patched in — and add a pointer to the “hole” into a global table in a different assembly section, along with an id for the specialized instruction and the patch-in case (unconditional branch, branch-and-link, branch-if-less-than-zero...).

(Macro-expanded) GNU C, simplified

```c
asm goto (".pushsection .data, 42"
" .quad hole_to_fill_%=%=
" .quad " SPECIALIZED_INSTRUCTION_ID "
" .quad " PATCH_IN_CASE "
".popsection"
"hole_to_fill_%=%="
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Patch-ins in action

The assembly section containing the global table is scanned to compute the addresses to patch within replicated code.

Jumps generated this way, and some inline `asm` for conditional branches, can make VM branches optimal on a given architecture.

[Demo: disassembling and timing the down-counter under no-threading dispatch]
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What should I call this?

Am I still speaking of efficient interpreters, or have I already crossed into JIT territory? The answer may be blurry, particularly with respect to common public expectations.

I will avoid the question, and call the software a generator of efficient “virtual machines”.

My VM generator is called Jitter, and a VM generated by Jitter will be “Jittery”. You are free to follow your imagination in interpreting the name. Here are some possibilities:

- a software attempting to pass for a JIT without success
- a maker of JITs
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I’m releasing Jitter’s code right now, for the first time.

http://ageinghacker.net/projects/jitter/ghm-2017

There are rough edges but the code is not terrible. If you like languages you’ll have fun.

- I want to propose Jitter as a GNU project.
- Implementation-wise, rewrite rules are the most urgent thing. [I also have to actually use the Array; that’s easy and will be ready soon, possibly before the GHM is over. Hierarchical wrapped globals will have to wait a little.]
- I have to finish the manual. Of the already existing part I strongly recommend the section about when not to use VMs in the introduction.
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Thank you

Also thanks to the people from whose work I learned the bases on which I built Jitter, particularly Anton Ertl. See the bibliography on slide 71, and the NOTES file in the tarball.

My virtual machine is faster than yours.

Any questions?

Are you thinking of some application for Jitter? Tell me.
Bibliography I


Saiu, L. (2017). The Jitter NOTES file. The NOTES file in the current Jitter distribution contains my (crudely) annotated bibliography, originally intended just for myself, with many more references. Not really a literature review, but at least a list of useful pointers to scientific publications.